Appl. No. 10/734,905
Amdt. dated September 27, 2005
Reply to Office Action of March 11, 2005 and the Notice of
Non-Compliant Amendment mailed September 22, 2005

PATENT

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1   1.   (Currently Amended) A method of computer aided design comprising:

2   providing a description of a first logic function using a high-level design

3   language;

4   synthesizing gates to obtain a first alternative netlist for the first logic function;

5   performing a technology mapping of the first alternative netlist to obtain a first

6   mapping netlist;

7   synthesizing gates to obtain a second alternative netlist for the first logic function;

8   performing a technology mapping of the second alternative netlist to obtain a

9   second mapping netlist;

10   selecting one of corresponding first mapping netlist or second mapping netlist

11 based on a comparison of the first mapping netlist with the second mapping netlist based on

12 design criteria, wherein the selected one of the corresponding first mapping netlist or second

13 mapping netlist is a selected mapping netlist;

14   optimizing the selected mapping netlist; and

15   performing a technology mapping on the ~~second~~ selected mapping netlist after

16 optimizing, wherein the first mapping netlist comprises digital signal processing blocks.

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2   2.   (Previously Presented) The method of claim 1 wherein the design criteria

3   includes optimizing for area.

1   3.   (Previously Presented) The method of claim 1 wherein the design criteria

2   includes optimizing for delay.

1   4.   (Previously Presented) The method of claim 1 wherein the first mapping

2   netlist comprises look-up table structures.

1   5.   (Cancelled)

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1   6.   (Previously Presented) The method of claim 1 wherein the first alternative

2 netlist comprises logic gates.

1   7.   (Currently Amended) The method of claim 1 wherein the step of

2 performing a technology mapping of the first alternative netlist to obtain a first mapping netlist is

3 done on a copy of the first alternative netlist.

1   8.   (Currently Amended) A method of logic synthesis comprising:

2   generating a first alternative netlist for a logic function;

3   generating a second alternative netlist for the logic function, wherein the second

4 alternative netlist has a different gate configuration from the first alternative netlist; and

5   selecting one of the first alternative netlist or the second alternative netlists as a

6 selected alternative netlist based on results of a technology mapping of the first alternative netlist

7 and the second alternative netlists, wherein the first alternative netlist includes a digital signal

8 processing block.

1   9.   (Previously Presented) The method of claim 8 further comprising:

2   performing a synthesis optimization on the selected alternative netlist to obtain an

3 optimized selected alternative netlist.

1   10.   (Previously Presented) The method of claim 8 further comprising:

2   performing a synthesis optimization on the selected alternative netlist to obtain an

3 optimized selected alternative netlist; and

4   performing a technology mapping on the optimized selected alternative netlist.

1   11.   (Currently Amended) The method of claim 8 wherein the selecting one of

2 the first alternative netlist or the second alternative netlists is based on area.

1   12.   (Currently Amended) The method of claim 8 wherein the selecting one of

2 the first alternative netlist or the second alternative netlists is based on depth.

1   13.   (Currently Amended) A method of logic synthesis comprising:

2   generating a netlist for a logic function;

3   performing a first technology mapping on the netlist;

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4   after the first technology mapping, performing a synthesis optimization on the

5   netlist; and

6   after the synthesis optimization, performing a second technology mapping on the

7   netlist, wherein the first technology mapping includes a digital signal processing block.

1   14.   (Previously Presented) The method of claim 13 wherein the first

2   technology mapping maps the netlist to the same target technology as the second technology

3   mapping.

1   15.   (Previously Presented) The method of claim 13 wherein the logic function

2   is provided in a high-level design language.